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(PTO/SB/05 and PTO/SB/06)

Case Docket No. WAB 98553
Date: September 23, 1999

ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Dear Sir/Madam:

Transmitted herewith for filing is the patent application of:

Inventor(s): Philip J. Calamatas

For: ***DATA BUS MEMORY CIRCUIT***

X Specification (10 Pages), Claims (2 pages), Abstract (1 page) and (2 sheet(s)) of Informal Drawings)

X Declaration and Power of Attorney

___ An Assignment of the Invention to _____

___ An Information Disclosure Statement

___ A Certified Copy of _____ application(s) No.(s) _____

___ A Verified Statement to establish Small Entity status under 37 CFR 1 9 and 37 CFR 1.27

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X A Filing Fee, calculated as shown below:

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BASIC FEE	[redacted]	[redacted]	[redacted]	$ 380	or	[redacted]	$ 760
TOTAL CLAIMS	3-20=	*0	x 9=	$	or	x18=	$
INDEP CLAIMS	2- 3=	*0	x39=	$	or	x78=	$
MULTIPLE DEPENDENT CLAIM PRESENTED			+130=	$	or	+260=	$
			TOTAL	$	or		$ 760

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Respectfully submitted,
JAMES RAY & ASSOCIATES

Elroy Strickland

By: Elroy Strickland
Attorney For Applicant(s)
Reg. No. 22,546

2640 Pitcairn Road
Monroeville, PA 15146

Telephone: (412) 380-0725
Facsimile: (412) 380-0748

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Susette Doherty

DATA BUS MEMORY CIRCUIT

CROSS-REFERENCE TO RELATED Application

This application relates to co-pending Provisional Application Serial No. 60/109,951, filed on November 25, 1998 and entitled "Intelligent Door Controller Unit. This Provisional Application is assigned to Westinghouse Air Brake Company, the assignee of the present application and is incorporated herein by reference thereto.

FIELD OF THE INVENTION

The present invention relates, in general, to memory circuits and, more particularly, this invention relates to the details of a simple, self-locking memory circuit for a tri state bit line of a data bus.

BACKGROUND OF THE INVENTION

In the above-noted provisional application, a self-locking circuit is shown connected to a tri state bit line of a data bus interconnecting a CPU and other digital transceiving processing devices, such as a Motion Control Digital Signal Processor (DSP), to provide a memory of the last data value or electrical potential sent on such line, i.e., the last read or write transfer, and low impedance state between the CPU and the processing devices. The line, or more correctly, the data on the line is said to be "tri state" because of the three states at which data operate, namely, a high and a low voltage state and a state in which no current flow is generated.

The self-locking circuit of the invention is useful on any connecting bit line where it is desirable to latch and hold the last value or state on the line and thereby retain and maintain such value once the driver relinquishes control of the line, i.e., when the line returns to a high impedance state.

SUMMARY OF INVENTION

The present invention uses a known, commercially available, non-inverting, non-clocking buffer amplifier chip and a simple parallel resistor connected across the chip, i.e., connected to the input and output terminals of gates of the chip. These two means (chip and resistor) when connected to a tri state bit line provide a predetermined relatively high impedance on the line that is effective in latching the latest value found on the line.

More particularly, a circuit device supplying the bit line with a signal has a relatively low impedance. The relatively low impendence of the supply device and the relatively high impedance of the latching circuit of the invention provides a voltage divider that produces a low voltage at the supply circuit while the high impedance of the latching circuit develops a relatively high voltage.

When the signal from the supplying circuit goes from a low state to a high state, the output voltage of the latching circuit is at a low state. Thus, the input voltage to the amplifier chip and resistor of the invention initially rises to the voltage divided level. At a certain voltage threshold the latching circuit switches to the high state, with the output terminal of the chip

now also being in a high state. The latching circuit now has essentially the same high state of the output of the supplying (sending) circuit.

Since the chip has no clocking elements, it is stable over time and holds the value received from the sending circuit. It will not switch until such time as a new value is imposed on the input terminal of the latching circuit at a level that moves through a low voltage threshold value to return the circuit to a low state. Again, the circuit will hold this "low" value until it is forced to change by a new "high" state sent on the bit line and imposed upon the latching circuit.

In the above incorporated patent application, for example, the timing structures of the CPU and DSP are different. By holding data over time, the circuit of the present invention allows the CPU and DSP to work together while simultaneously preventing noise on the bit line from being transferred between the CPU and DSP, i.e., the impedance of the circuit of the invention temporally changes (lowers) only when the latest value or state on the bit line builds or lowers to a current level above or below threshold levels of the circuit after which the chip of the circuit conducts. When this occurs, the impedance of the circuit temporarily falls to a low value, temporarily loads the line, then returns to the relative high impedance value to hold the new, latest value and to remove the load from in the line. In this manner, the circuit is self-locking and resists transferring noise and electromagnetic

interference as such noise and interference do not sustain current levels sufficient to force the switching of the circuit.

OBJECTS OF THE INVENTION

It is, therefore, one of the primary objects of the present invention to provide a simple digital latching circuit for retaining the latest information (high or low state) conveyed on a bit line.

Another object of the present invention is to provide a data latching circuit that requires no clocking, timing or synchronization pulses to latch the data.

Yet another object of the present invention is to provide a means for testing the integrity of a printed circuit board bus signal.

Still another object of the present invention is to use a commercially available, non-inverting digital amplifier chip and an electrical resistor connected across the chip as the latching circuit of the invention and in which the chip and resistor provide a predetermined impedance for such latching circuit.

A further object of the present invention is to provide a digital circuit having the capability of extending the hold times of data conveyed on bit lines connected between digital circuit devices.

Yet another object of the present invention is to provide a circuit which exhibits a substantial reduction in noise and interference for tri state digital bit lines.

In addition to the specific objects and advantages of the present invention described above, various other objects and advantages of the invention will become more readily apparent to those persons who are skilled in the relevant memory circuit art from the following more detailed description of the invention, particularly, when such description is taken in conjunction with the attached drawing Figures and with the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic diagram of eight buffer memory, latching circuits of a presently preferred embodiment of the invention and their connection to bit lines of an eight bit data bus; and

Figure 2 is a circuit diagram useful in explaining the operation of such presently preferred embodiment of the circuit of the invention.

BRIEF DESCRIPTION OF A PRESENTLY PREFERRED EMBODIMENT

Reference is now made, more particularly, to the drawings. Figure 1 thereof shows eight buffer memory circuits, generally designated 220, electrically connected, respectively, to eight tri state bit lines 1 to 8 of a data bus 9 interconnected between tranceiving digital components 20 and 30. An example of such an interconnection of components is the CPU 230, the Digital Signal Motion Control Processor (DSP) 320 and the Complex Programmable Logic Devices (CPLD) 300 interconnected in the read/write manner shown in Figures 7B and 10B of the above incorporated patent application.

The buffer memory circuit of the invention bears the same reference numeral (220) found in the above application. The buffer memory of the present invention, however, has utility on any data bus or digital circuit where memory of the last transfer of data requires retention and can be used on any number of bit lines.

The eight circuits 220 which are illustrated in Figure 1 are substantially identical so that only one of the circuits is discussed herein in detail. This circuit is shown, in Figure 2 of the drawings, connected to a bit line 4 extending between the two digital circuits 20 and 30.

More particularly, circuit 220 of the invention comprises a digital buffer amplifier chip 10 and a parallel resistor 12 connected across the chip 10 such that the input and output terminals 14 and 16 of the chip 10 (only schematically shown in the figures) are connected together by the resistor. Chip 10 is a well known, commercially available, non-inverting digital amplifier having no clocking elements. Its input terminal 14 is connected to a bit line, namely, bit line 4 in Figure 2. As such, in the circuit 220, the signal or potential newly applied to input 14 of the chip 10 from the bit line is retained after current in the line builds to a predetermined threshold level of circuit 220.

The circuit operates in the following manner:

The input to circuit 220, in Figure 2, is received from a digital circuit device represented schematically by an amplifier symbol 20 and a resistor 22. Resistor 22 represents the internal output impedance of amplifier 20 and is determinative of its output

voltage. The electrical output impedance of amplifier 20 is relatively low in comparison to that of resistor 12 of latching circuit 220 such that any voltage developed by amplifier 20 divides at the connection 24 of the two resistors 22 and 12, with the greater of the two voltages being developed across resistor 12.

For example, if amplifier 20 produces a five volt signal, it can divide on a one and four volt basis, with the four volts being applied to the input terminal 14 of chip 10. The present state of chip 10, however, may be at zero volts, i.e., zero volts at its input and output terminals 14 and 16. Output terminal 16 and a series resistor 26, which represents the internal impedance of chip 10, are a virtual ground or virtual Vcc for circuit 220. Resistances 12 and 26 represent the total impedance of circuit 220 of the invention.

In the case of amplifier 30, as schematically presented, a resistor 32 is shown in Figure 2 that represents the internal impedance of the amplifier 30.

Circuit 220 has a voltage threshold level that permits the circuit to change states. If the divided voltage is at the threshold level, circuit 220 switches to a state where its input and output terminals 14 and 16 are now at a "high" state, such as the above divided four volt level. This occurs by chip 10 momentarily conducting, thereby momentarily loading the bit line, bit line 4, for example. As soon as the chip 10 conducts and goes "high", conduction and loading of the bit line 4 ceases. Being a

non-inverting device, chip 10 does not change the state or potential of the latest signal applied thereto.

In the drawing figures, amplifier symbol 20 is shown as a tri state bus driver but it is also a tri state receiver, as indicated by a second amplifier symbol 20A. The third amplifier (symbol 30) is also a bus receiver and driver, the dual function being again indicated by a second amplifier symbol 30A. In the read/write arrangement of the CPU and DSP in the above noted provisional application, the driver/receiver functions are interchangeable such that amplifier 30 can be the driver and amplifier 20 the receiver. In either case, circuit 220 holds the latest potential supplied on the bit line until one of the two, upper and/or lower thresholds of circuit 220 are crossed.

In crossing the lower threshold of circuit 220, amplifier 20 or 30 will place a "low" potential on the bit line while the other circuit is in a high state. Circuit 220, which is presently latched in a high state, tries to maintain the high state. However, when the voltage on input terminal 14 of chip 10 drops through the low threshold before the chip 10 conducts and switches to the low state, the chip 10 temporarily and monetarily loads the bit line 4. As the output 16 of the chip 10 changes state, the chip 10 immediately thereafter ceases conducting, unloads the bit line 4 and holds the new "low" state until such time that its upper threshold is reached, which occurs when a "high" voltage is received at input terminal 14.

Circuit 220 loads the bit line only when it switches (i.e. when chip 10 conducts) which makes the circuit 220 highly effective in resisting electromagnetic noise and interference, as such noise and interference can not sustain current flow and a voltage level sufficient to reach the switching thresholds of the circuit 220.

Further, the circuit 220 does not oscillate, as there is no phase shift between the input 14 and output 16 of chip 10 and does not hunt as the circuit 220 is a digital device having only high and low states. Rather, the circuit 220 latches and locks itself until its thresholds, high and low, are reached by a new state on the bit line.

In this manner, circuit 220 retains the latest information until it is forced to change, as per above. If the circuit 220 does not retain the last bit of information (potential), it is an indication of current leakage on the circuit board (not shown) on which chip 10 and resistor 12 are mounted. Circuit 220 thereby provides, in addition, an internal diagnostic function on the board. It alerts a technician of such a problem so that he or she can proceed to find the location of the leakage.

Because the circuit 220 extends hold times of data, it functions to match the timing of respective devices interconnected by bit lines that transfer data, such as the amplifiers 20 and 30, or the CPU and DSP devices described in the above incorporated patent application. As noted, above the CPU and DSP do not have a one hundred percent match in their timing requirements.

While the presently preferred embodiment for carrying out the instant invention has been set forth in detail, those persons skilled in the digital circuit art to which this invention pertains will recognize various alternative ways of practicing the invention without departing from the spirit and scope of the patent claims appended hereto.

What is claimed is:

1. A self-locking memory circuit for a tri state data bus having multiple bit lines, said self-locking memory circuit comprising:

a non-inverting buffer chip for connection to one of said bit lines;

a resistor having a predetermined electrical resistance connected across said buffer chip; and

said chip and resistor having upper and lower voltage thresholds that cause said chip to change states when a level of voltage applied to said chip and said resistor passes through said thresholds.

2. A programmable system comprising:

a Digital Signal Processor for transceiving discrete electrical inputs;

a tri state data bus electrically connecting said Digital Signal Processor to a CPU;

said Digital Signal Processor and said CPU having difference rates at which they operate in performing their respective functions, and

self-locking data bus circuits connected to respective bit lines of said data bus for matching different operating rates of said Digital Signal Processor and said CPU.

3. The programmable system, according to claim 2, wherein said system further includes:

a Complex programmable logic device for transceiving discrete electrical signals;

tri state data buses electrically connecting said Complex Programmable Logic Device to said CPU and said Digital Signal Processor, said Complex Programmable Logic Device and said Digital Signal Processor having rates at which they operate in performing their respective functions that are different from that of said CPU; and

self-locking data bus circuits connected to respective bit lines of said tri state data buses for matching different operating rates of said Complex Programmable Logic Device and said Digital Signal Processor with that of said CPU.

ABSTRACT

A self-locking memory circuit for a tri state data bus having multiple bit lines. The circuit includes a non-inverting buffer chip for connection to each bit line and a resistor having a predetermined electrical resistance connected across the buffer chip. The chip and resistor provide a predetermined impedance to the flow of electrical current in the self-locking circuit. The circuit changes its state when the current of the latest information on a bit line builds or lowers above or below threshold levels of the self-locking circuit.

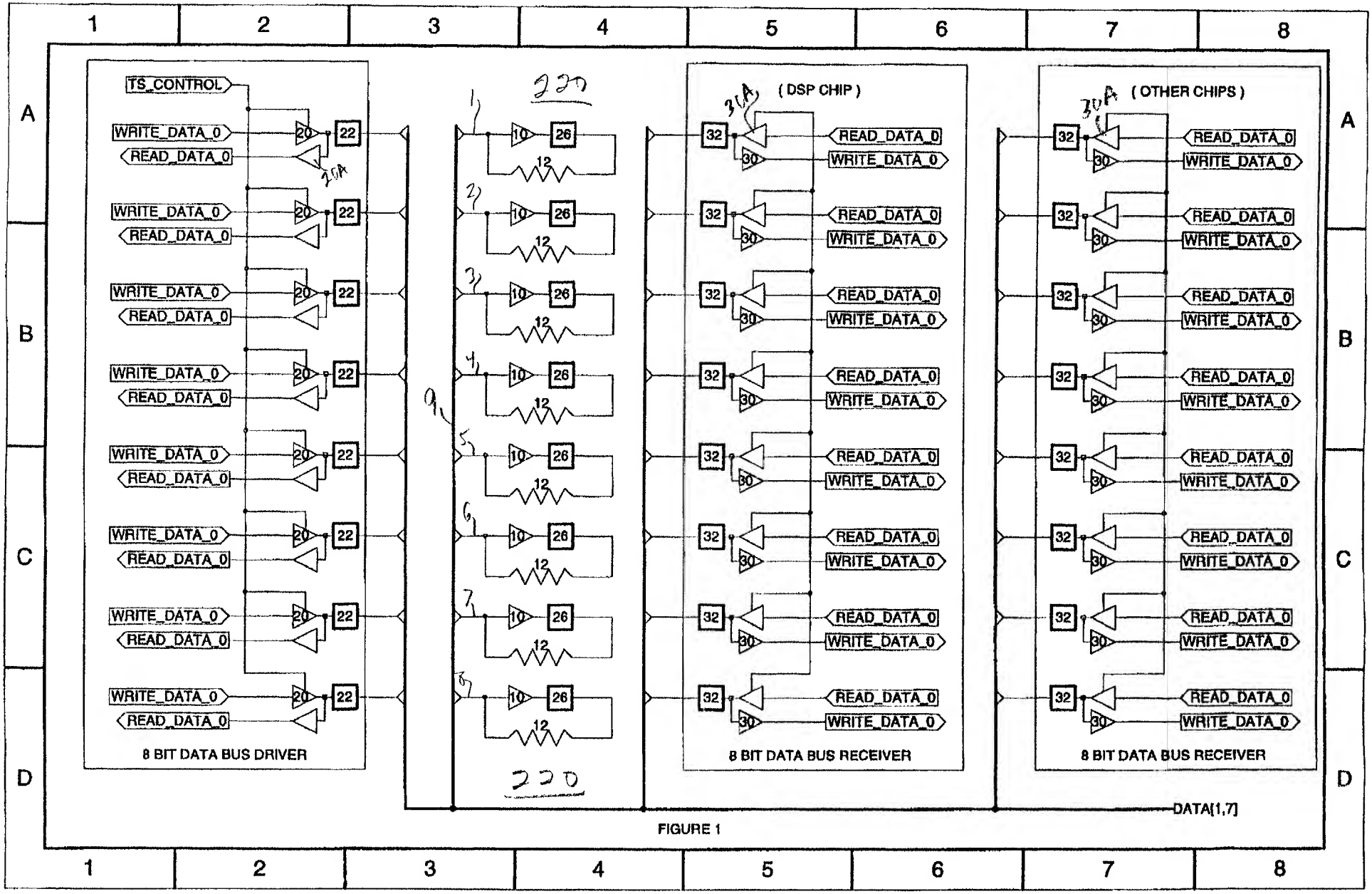

FIGURE 1

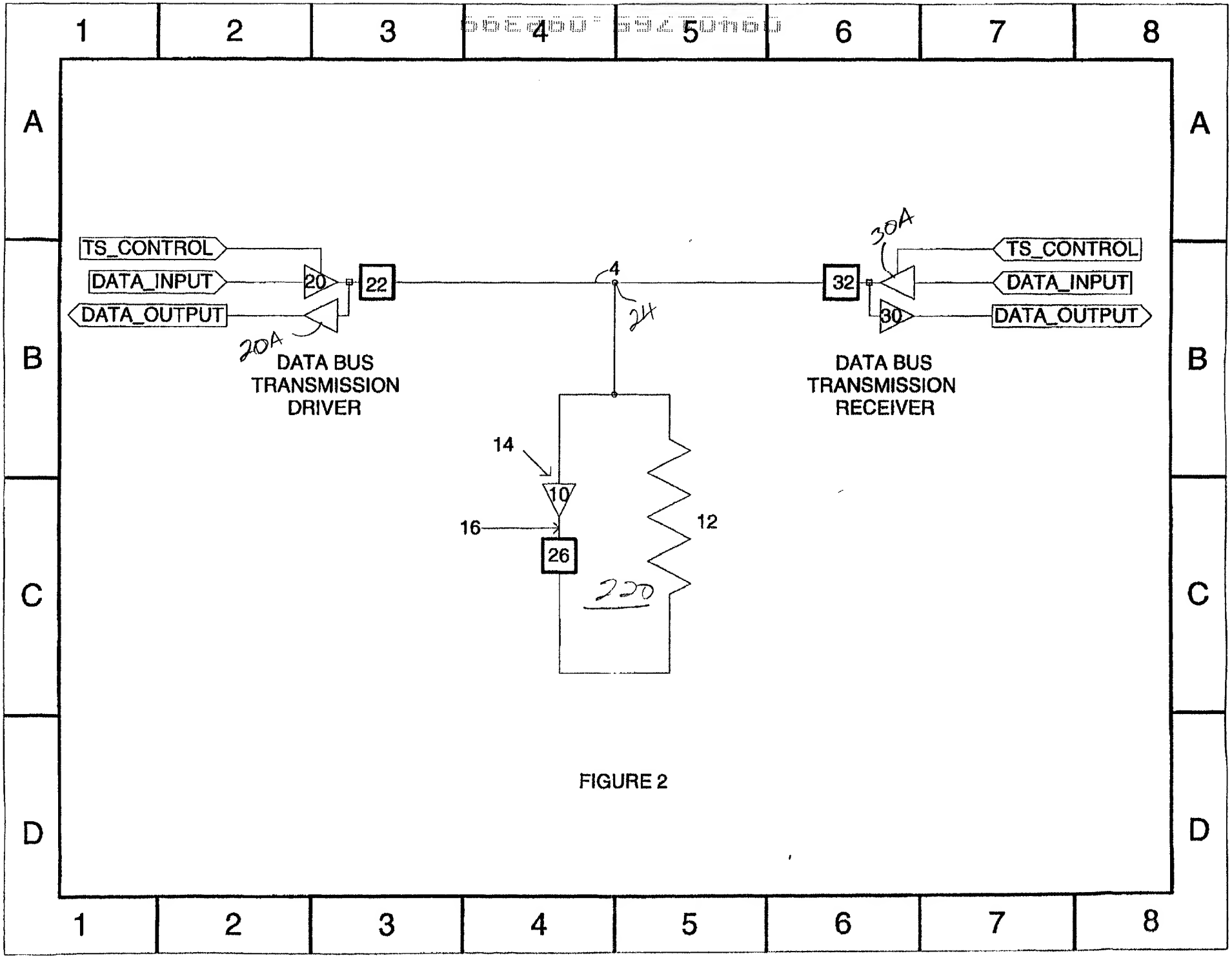

FIGURE 2

Attorney Docket NWAB 98440o WAB 98553

Declaration For U.S. Patent Application

(PTO/SB/01)

As a below named inventor, I hereby declare that·

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled.

DATA BUS MEMORY CIRCUIT

the specification of which (Check one of blocks 1, 2 or 3)

1. [X] is attached hereto.
2. [ ] was filed on _____ as International PCT Application Serial No _____
   and was amended on _____. (if applicable).
3. [ ] was filed on _____ as U.S. Application Serial No. _____
   and was amended on _____.(if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification. including the claim(s), as amended by any amendment referred to above

I acknowledge the duty to disclose information which is material to patentability as defined in 37 C F R 1 56

I hereby claim foreign priority benefits under 35 U S C 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed

List of Prior Foreign Applications (if applicable)

(Application Number)	(Country)	(Day/Month/Year Filed)	CERTIFIED COPY ATTACHED?
			[ ] Yes [ ] No
			[ ] Yes [ ] No
			[ ] Yes [ ] No
			[ ] Yes [ ] No

[ ] Additional foreign application numbers are listed on the attached sheet, PTO/SB/02B - Supplemental Priority Data Sheet or similar sheet

I hereby claim the benefit under 35 U S C 119(e) of any United States provisional application(s) listed below

List of U.S. Provisional Applications (if applicable)

(Application Number)	(Day/Month/Year Filed)

[ ] Additional provisional application numbers are listed on the attached sheet, PTO/SB/02B - Supplemental Priority Data Sheet or similar sheet

I hereby claim the benefit under 35 U S C 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U S C 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 C F R 1 56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

List of U.S. Parent Application Or PCT Parent Numbers (if applicable)

(Number)	(Day/Month/Year Filed)	(Status: Abandoned; Pending; Patent Number, if applicable)

[ ] Additional U.S. or PCT international application numbers are listed on the attached sheet, PTO/SB/02B - Supplemental Priority Data Sheet or similar sheet

And I hereby appoint as principal attorneys and agents, James O. Ray, Jr., Reg. No. 27,666; Forest C. Sexton, Reg. No. 22,054; Edmond S. Miksch, Reg. No. 38,558; James R. Stevenson, Reg. No. 38,755; John B. Sotak, Reg. No. 20,529; Gary J. Falce, Reg. No. 29,304; Elroy Strickland Reg. No. 22,546; Amos Bartoli, Reg. No. 42,299; Michele K. Yoder, Reg. No. 41,562 and Robert A. Shack, Reg. No. 29,976.

Please direct all correspondence to the following address:

JAMES RAY & ASSOCIATES
2640 PITCAIRN ROAD
MONROEVILLE, PA 15146

TELEPHONE: 412-380-0725
FACSIMILE: 412-380-0748

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true: and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 of Title and that such willful false statements may jeopardize the validity of the application or any patent issue thereon.

Full Name of Sole or First Inventor: Philip J. Calamatas

Inventor's signature: _____ Date: Sept 13/99

Residence: 3276 Carmina, Fabreville Laval Quebec, Canada H7P 4G9
(Street, City, State, Zip Code, Country)

Citizenship: Canadian

Post Office Address: 3276 Carmina, Fabreville Laval Quebec, Canada H7P 4G9

Full Name of Second Inventor: _____

Inventor's signature: _____ Date: _____

Residence: _____
(Street, City, State, Zip Code, Country)

Citizenship _____

Post Office Address _____

Full Name of Third Inventor: _____

Inventor's signature: _____ Date: _____

Residence: _____
(Street, City, State, Zip Code, Country)

Citizenship _____

Post Office Address _____

Full name of Fourth Inventor: _____

Inventor's signature: _____ Date: _____

Residence: _____
(Street, City, State, Zip Code, Country)

Citizenship _____

Post Office Address _____

[ ] Additional inventors are listed on the attached sheet, PTO/SB/02A - Supplemental Additional Inventor(s) Sheet or similar sheet